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**Workshop1**

Clock Dividers

1. The period of the clk\_en signal is 1.31 ms. The figure is shown below:

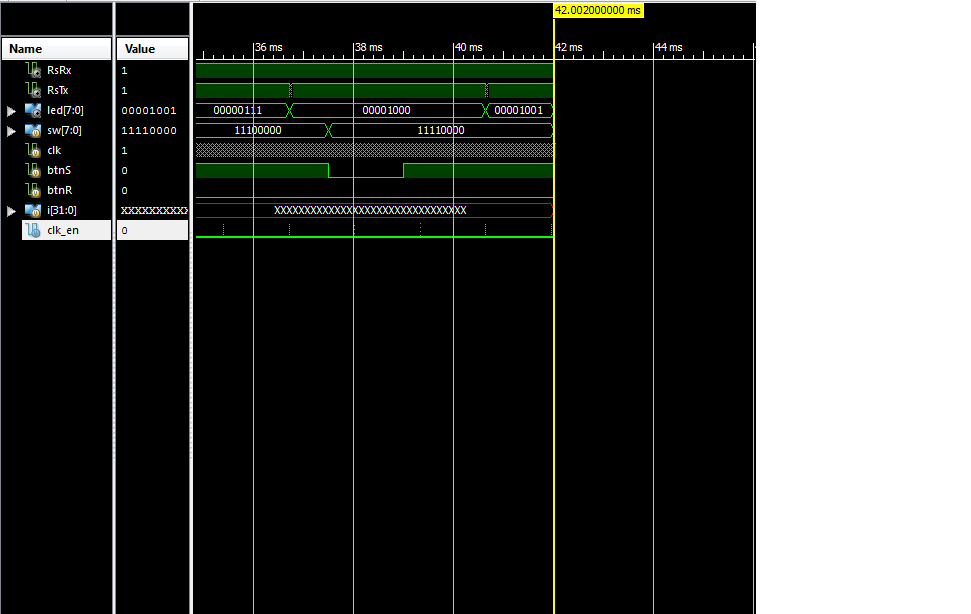


Figure 1: A waveform picture that captures rising edges of clk\_en

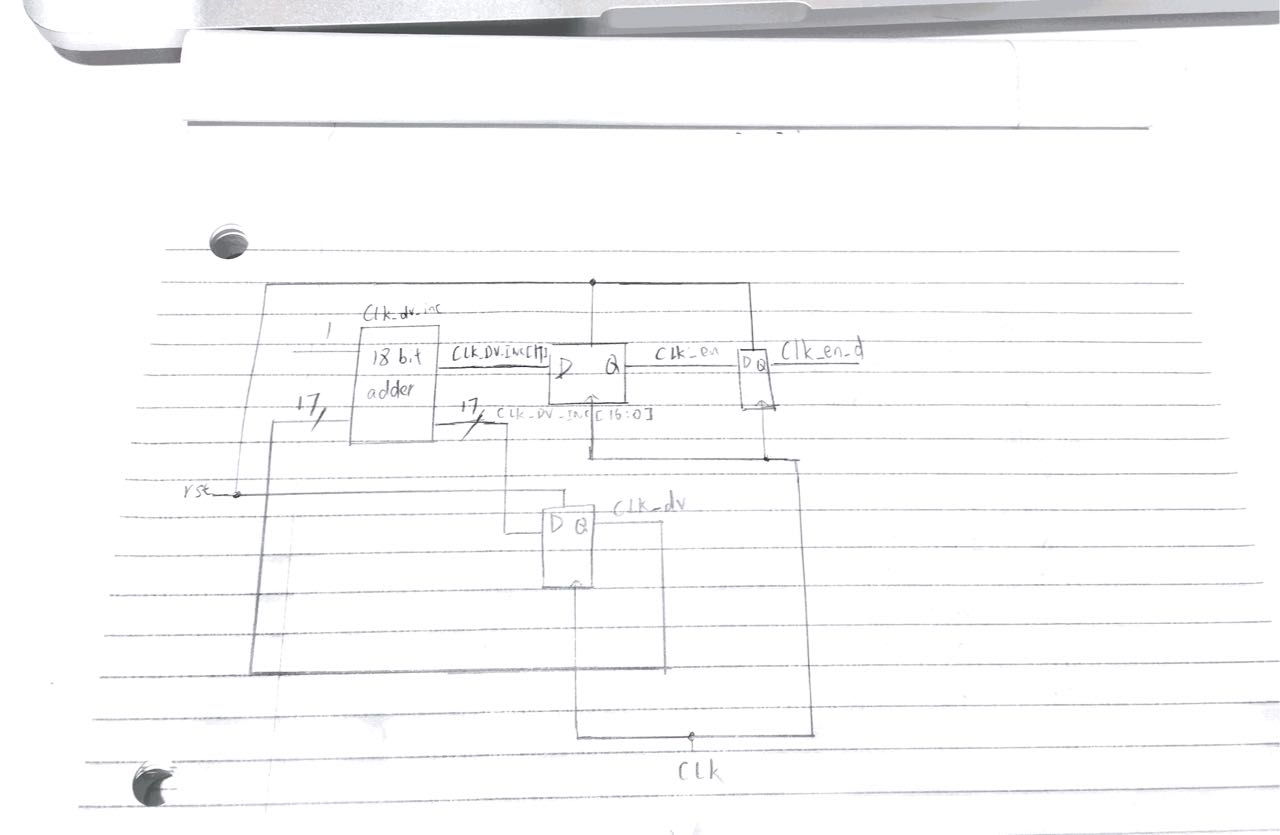
1. We have P = 1.31ms, and T = 10ns.
2. The value of clk\_dv signal is 0 when clk\_en is high.
3. 

Figure 2: Diagrams of clk\_dv, clk\_en and clk\_en\_d

Debouncing

1. This expression is used to record whether the button was pressed one cycle ago. The value of step\_d cam be changed only when clk\_en is 1, and it’s updated in the next cycle since it’s sequential logic. However, in the next cycle, clk\_en already becomes 0. So, ~step\_d[0] & step\_d[1] & clk\_en will always be evaluated to 0. clk\_en\_d is the clk\_en signal delayed by one cycle. When clk\_en\_d is 1, step\_d has already been updated, so we can determine whether the button was pressed or not one cycle ago.

1. It will not make the duty cycle 50%. In the old case, the clk\_en signal is high for very short an interval because once the clk\_dv\_inc[17] becomes 1, clk\_dv becomes will become 0. Then clk\_dv\_inc will be reset to 1 and clk\_dv\_inc[17] becomes 0 again. So, clk\_en is 1 every cycles. If we use clk\_en <= clk\_dv[16] instead, clk\_en signal will remain 1 for a much longer time because when clk\_dv[16] becomes 1, clk\_dv\_inc won’t be reset immediately. So, clk\_en will remain 1 until clk\_dv\_inc[17] becomes 1. It’s nearly half of the total cycle time. So, the duty cycle will become much larger instead of 50%.

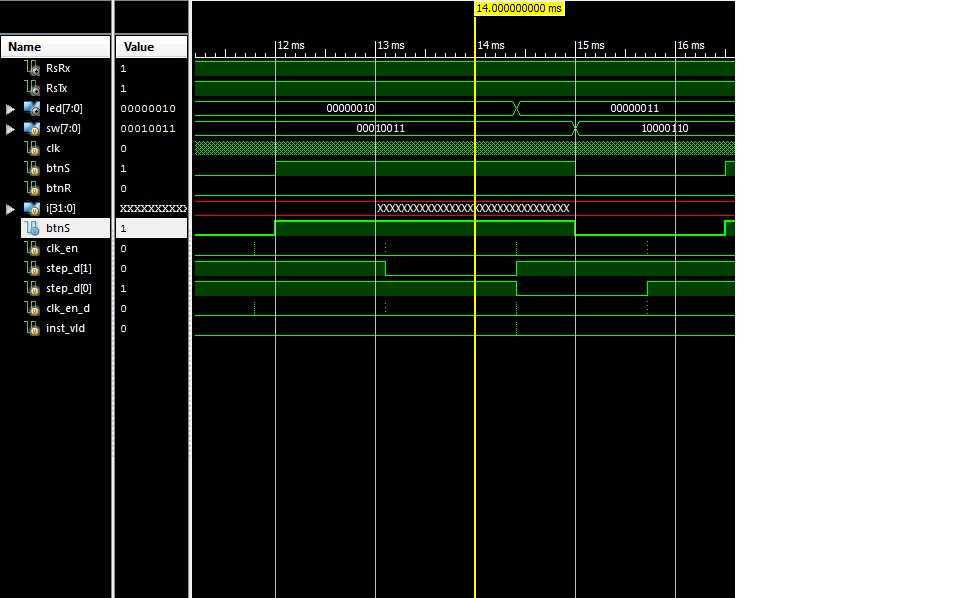


Figure 3: Timing relationship of signals

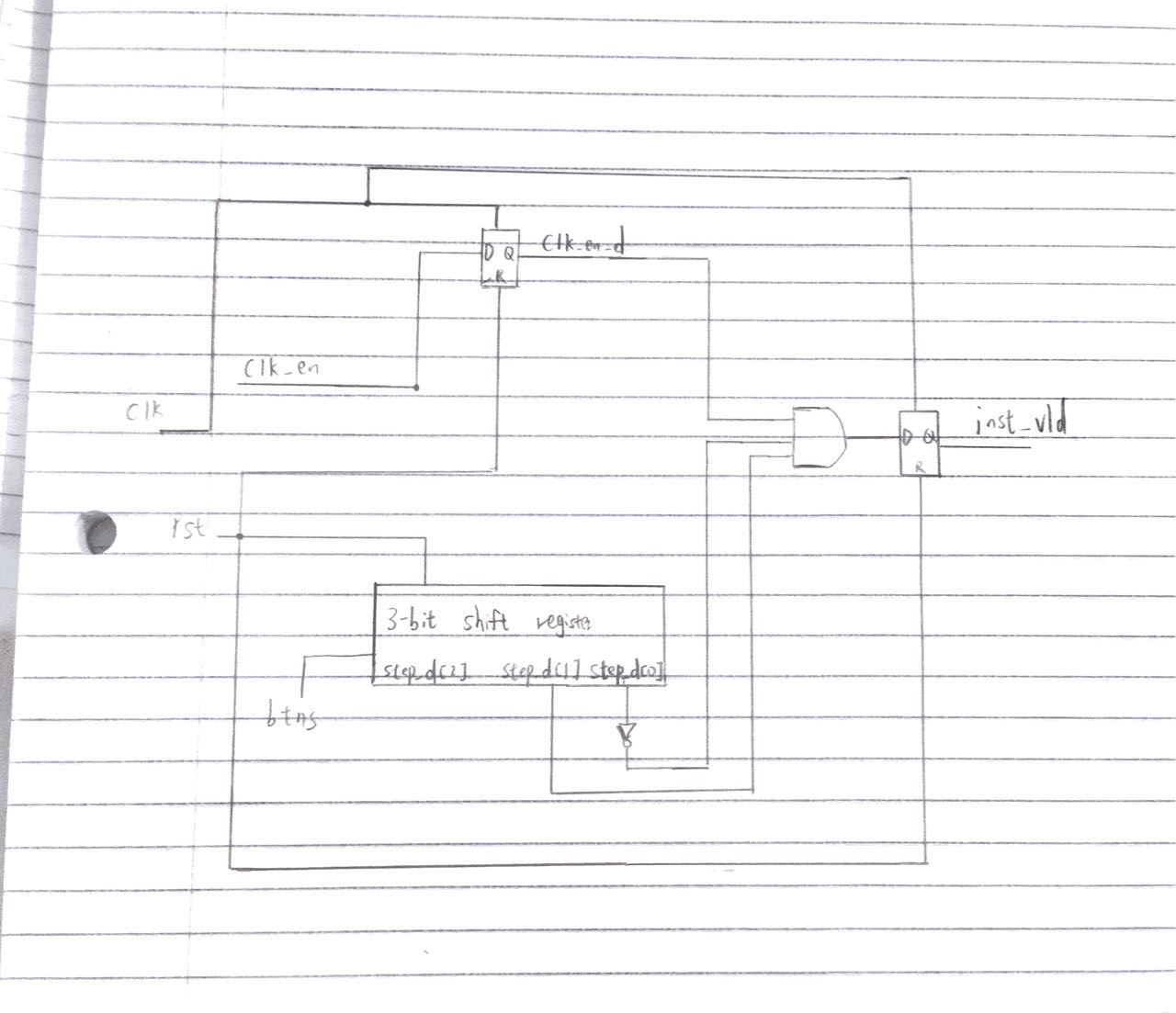


Figure 4:Diagram of signals

Register File:

1. Line 33: rf[i\_wsel] <= i\_wdata. This is sequential logic. Because this line uses <=, it indicates that this expression uses a non-blocking assignment; the register is written on the positive clock edge.
2. Line 35 and 36:

assign o\_data\_a = rf[i\_sel\_a];

assign o\_data\_b = rf[i\_sel\_b];

This is combination logic. We can use multiplexers to manually implement.

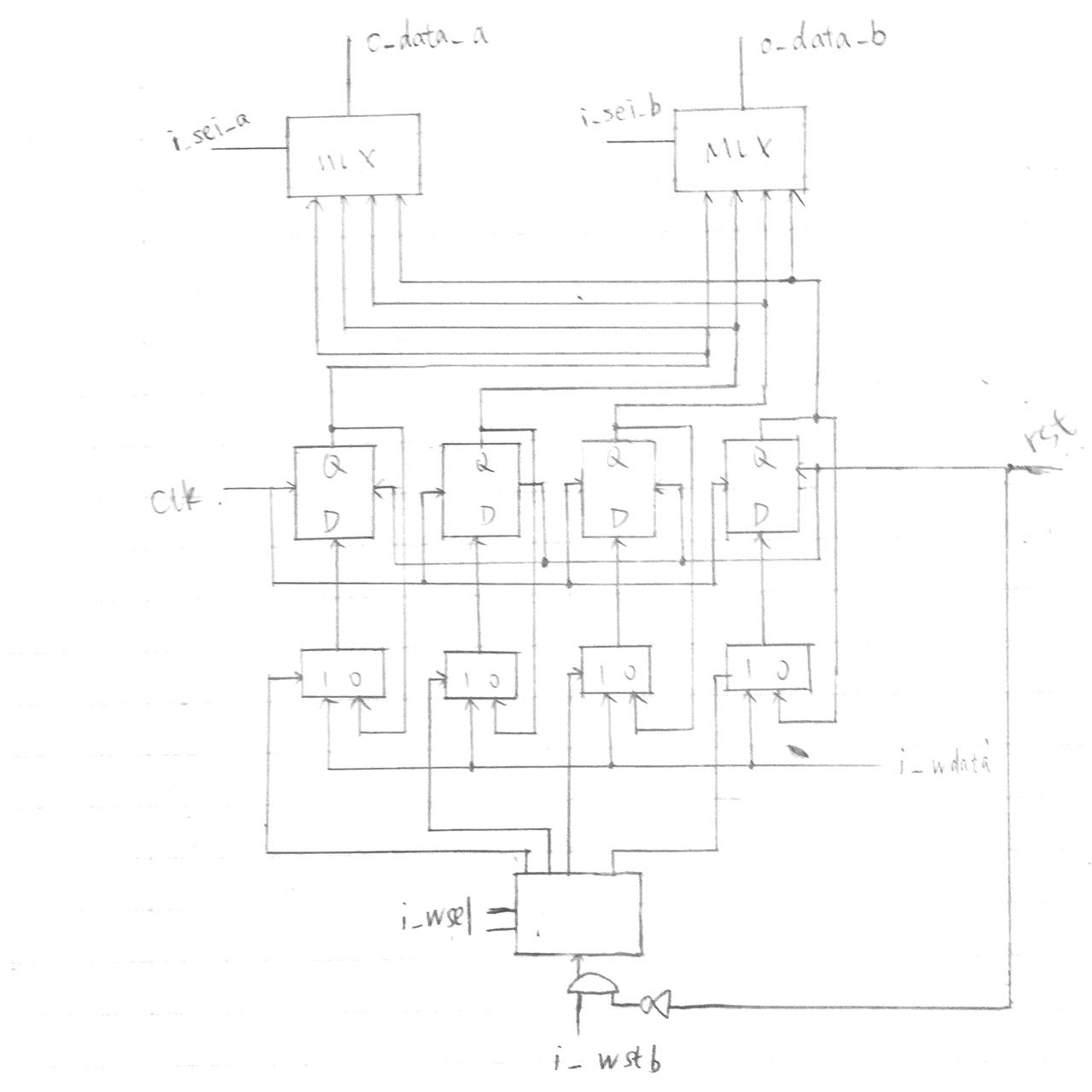


Figure 5: Circuit diagram of register files

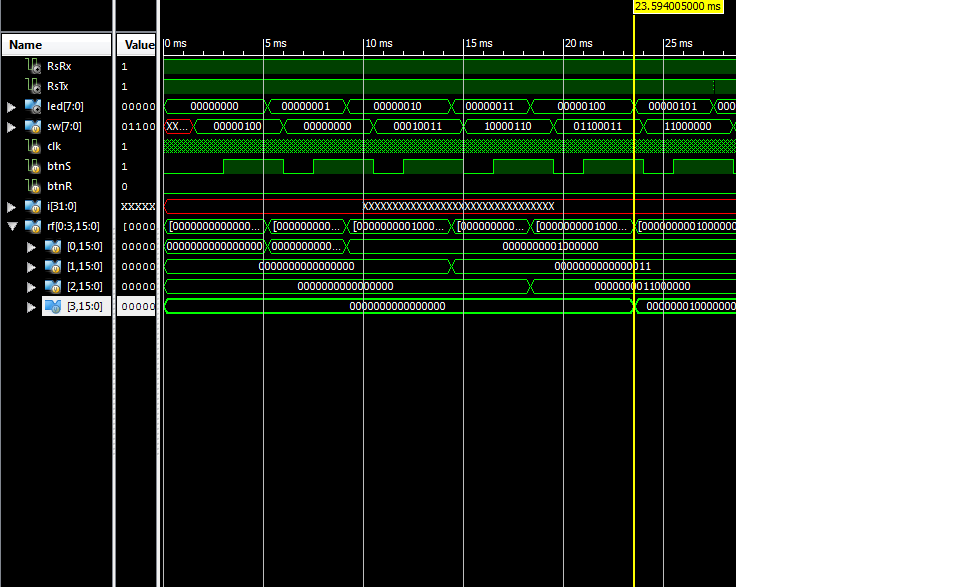


Figure 6: Waveform of the first time register 3 is written with a non-zero value